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(54) DC to DC converter.

(57) An improved DC to DC converter is provided in particular for converters with high power density requirements. The converter comprises an input voltage source and a capacitor connected in series to the voltage source. A switching transistor configuration connects the voltage source and the capacitor alternatively to the primary windings of a transformer. The secondary windings of the transformer are connected to a full-wave rectifier and a filter. The output voltage provided at the output of the filter is modulated by a controlling means.

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BACKGROUND

Field of Invention

This invention applies to the field of DC to DC power conversion and in particular to converters required to provide high power density.

Prior Art

A vast variety of topologies have been invented over the years with the purpose of improving power density of power converters. Some of these topologies provide means to reduce or to eliminate switching losses in order to allow increased frequency of operation, increased efficiency, reduced size and weight. Typical of this approach is the technique disclosed in Patent No. 4,415,959, issued to P. Vinciarelli, for "Forward Converter Switching at Zero Current" which reduces the size of the energy storage components.

Another approach is disclosed by U.S. Patent No. 4,618,919, issued to Hubert C. Martin, Jr., for "Topology for Miniature Power Supply with Low Voltage and Low Ripple Requirements". This patent combines two single ended (flyback) converters to increase effective ripple frequency and reduce the size of energy storage components.

Another approach is to maximize the energy of switching devices and the transformer in order to improve the power transfer characteristics of the converter as indicated in U.S. Patent No. 4,441,146 issued to P. Vinciarelli for "Optimal resetting of the transformer's core in single ended forward converters" and in U.S. Patent No. 4,809,148 issued to Barn for "Full-fluxed, single ended DC converter".

Finally, in an article published in the PCIM magazine, January 1991, p. 8, "New PWM Topology features zero- voltage switching and constant switching frequency", and also disclosed in U.S. Patent No. 4,959,764, John A. Bassett proposes a topology that offers both the improved utilization of components and lossless switching, thereby allowing efficient operation at high frequency. While each of the above disclosures addresses some facets of the power conversion issue, none provides an approach achieving all of the advantages discussed above.

Summary of the Invention

This invention introduces a topology featuring the following characteristics:

- Low voltage stresses on both switching devices and output rectifiers.
- Low ripple voltage.
- Inherent capability of operating with zero voltage switching.
- Optimal utilization of the magnetic materials used in the circuit.

All of the above principal characteristics are achieved by merging a bidirectional buck boost converter and a double ended, buck derived converter in a single power conversion structure.

Brief Description of the Drawings

Fig. 1a is a simplified circuit diagram illustrating features of one embodiment of the present invention.
Fig. 1b represents the wave diagrams of various components of Fig. 1a.
Fig. 2a is a circuit diagram illustrating features of another embodiment of the present invention.
Fig. 2b represents the wave diagrams of various components in Fig. 2a.
Fig. 3a is a circuit diagram illustrating features of still another embodiment of the present invention.
Fig. 3b is a circuit diagram of still another embodiment of the present invention.
Fig. 3c is a circuit configuration of a prior art topology.
Fig. 4a is a wave diagram of magnetizing currents for full load and no load conditions in Fig. 3b.
Figs. 4b and 4c depict the wave forms of switching transistor currents in Fig. 3b .
Fig. 4d is a wave diagram of the current in primary winding 32 in Fig. 3b.
Fig. 5a is the wave diagram of point A of Fig. 3a or 3b at no load.
Fig. 5b is a wave diagram of point A in Fig. 3a or 3b at full load.
Fig. 6 is a circuit diagram which illustrates another embodiment of the present invention.
Fig. 7 is a circuit diagram illustrating another embodiment of the present invention.
Fig. 8 is a circuit diagram illustrating still another embodiment of the present invention.

Description of the Preferred Embodiments

In the preferred embodiment of Figure 1a, a voltage source 14 supplies a voltage Vin to a flyback converter formed by a toggle switching device 12, a capacitor 16 of value C_1, and an inductor 10 of value L.

Switch 12 is assumed to be in position A for a time interval t_1, then instantaneously moves to position B for a time interval t_2. The process is repeated indefinitely with a period T given by:

$$T = t_1 + t_2 \quad (1)$$

Duty cycle D is defined as:

$$D = \frac{t_1}{T} \quad (2)$$

This action of switch 12 connects inductor 10 alternatively across the input voltage source 14 and cross capacitor 16 . Assuming that capacitor 16 has a value large enough such that the variation of the voltage V_{c1} acrosscapacitor 16 during a time interval T is negligible, its steady state value must satisfy the volt-second balance across inductor 10:

$$Vin.t_1 = V_{c1}t_2 \quad (3)$$

$$V_{c1} = Vin.\frac{t_1}{t_2} \quad (4)$$

By substituting (1) and (2) into (4) we get:

$$V_{c1} = Vin\frac{D}{1-D} \quad (5)$$

This is the familiar DC transfer function of the buck boost (flyback) converter. The important characteristic of this flyback converter is that due to the bidirectional nature of the switch 12, energy can flow from either voltage source 14 to capacitor 16 or vice versa during either position of the switch.

This is illustrated in Figure 1b, wherein the current flowing through inductor 10 is triangular and has zero average value, and the voltage across it is a square wave with a positive value V_{in} and a negative value Vc_1.

Referring now to Figure 2, a bridge rectifier 20 and a filter formed by inductor 22 with a value L_f and capacitor 24 with a value C_f are now connected across the inductor 10, with a resistor 26 loading the filter's output. The average output voltage Vo appearing across the load 26 is given by:

$$V_o = Vin.D + Vin\frac{D}{1-D}.(1-D) \quad (6)$$

or,

$$V_0 = 2VinD \quad (7)$$

The circuit of Figure (2) is illustrative of a principal feature of the invention while equation (7) shows its DC transfer characteristic, i.e., the value of its output voltage as a function of the input voltage and the operating duty cycle.

Switch 12, in addition to driving the bidirectional flyback converter, also operates as a double ended converter in conjunction with the circuit connected in parallel to inductor 10, generating the output voltage given by equation (7). The introduction of the loading circuit of Figure 2a which includes the full wave

rectifier 20, filter inductor and capacitor 22 and 24 and load resistor 26, alters the current in the flyback inductor 10 as discussed below.

Assuming that the filter inductor 10 is large enough such that its current i_L is ripple free, during interval t_2 this current will be extracted from capacitor 16. Consequently, the volt-second balance constraint on flyback inductor 10 will cause a DC current level buildup in it, thereby maintaining the voltage on capacitor 16 at the value given by equation (5). The current in inductor 10 under intermediate load and under full load is shown in Figure 2b. As is shown later, the situation where ΔI_{LPTP} has twice the value of the output current Io is of particular significance for zero voltage switching operation. Although the circuit of Figure 2a can be used as is, circuit configurations where the output voltage is isolated from the input circuit or at least is referred to the same ground find more applications.

One such circuit shown in Figure 3a can be obtained by using an isolation transformer 30 to connect the rectifier bridge 20, the filter 22-24, and the load 26 across the flyback inductor 10 .

At this point, a significant simplification may be obtained by eliminating inductor 10 and replacing it with the magnetizing inductance of the primary winding 32 of transformer 30, after gapping its core or using a core material capable of supporting the DC flux resulting from the DC current buildup mentioned before. It will be evident to those versed in the art that depending on the application, transformer 30 may be configured as an autotransformer and can have a center-tapped secondary or a multitude of secondaries if more than one output voltage is desired.

In order to contrast the advantages of this invention with the prior art, the preferred embodiment of Figure 3b can be compared to prior art circuits like the one disclosed in U.S. Patent 4,441,146. In Figure 3b, the toggle switch is realized using two MOS transistors 34 and 36, driven by two complementary signals so that when transistor 34 is on, transistor 36 is off and vice versa. Also, in order to avoid cross conduction, a short delay time is provided between the turn-off of one transistor and the turn-on of the next. This delay will have no impact on the operation as described above, since when transistor 34 is turned off, the current of the flyback inductor (now the shunt inductance of transformer 30) will free wheel through the body diode of 36 and vice versa.

For reference purposes, the circuit shown in U.S. Patent 4,441,146 at Figure 4e is shown herein in Figure 3c, this being one of several possible embodiments. The components 38 and 40 form a "magnetizing current mirror" that resets the core of the transformer. In this case, the magnetizing inductance of the transformer 42 is fulfilling no useful purpose. Presumably the magnetizing inductance is kept at the highest value possible in order to minimize magnetizing current and, as opposed to the circuit of the present invention, eliminates any DC component from the core flux at any operating condition. Otherwise, the circuit is a single ended forward converter, with an output voltage given as:

$$Vo = Vin.D \qquad (8)$$

Equation (8) assumes unity turns ratio for transformer 42.

Assuming that the converter is designed to operate over an input voltage range $Vin_{(min)}$ to $Vin_{(max)}$, corresponding to a duty cycle range D_{max} to D_{min}, the ripple voltage appearing across the filter inductor will have a maximum peak to peak value of:

$$V_{ptp(max)} = Vin_{max} \qquad (9)$$

In the converter of the present invention illustrated in Figure 3b, the peak-to-peak ripple will be the difference between the secondary voltage during the conduction of transistor 34 and the secondary voltage during the conduction of transistor 36. Assuming the same input voltage range and same output voltage, the transformer turns ratio has to be 0.5 (ref. eq. 7). The peak-to-peak voltage will therefore be:

$$V_{ptp(max)} = 0.5\left(Vin - \frac{VinD}{1-D}\right) \qquad (10)$$

or

$$V_{ptp_{(new)}} = \frac{0.5Vin(1-2D)}{1-D} \quad (11)$$

As we can see, the value of the voltage is a function of the duty cycle and it nulls at D = 0.5. Furthermore, assuming a practical range of D of 0.35 to 0.7 (an input voltage range of 2:1) the maximum peak to peak voltage will occur at the highest input voltage and will have the value:

$$V_{ptp_{(new)}} = 0.5 . Vin_{max} \frac{1-0.7}{1-0.35} = 0.2308Vin \quad (12)$$

This value represents an improvement of a factor of $V_{ptp(FWD)}/V_{ptp(NEW)}$ = 4.33. The significance of this result is that the filter inductor can be reduced by a factor of 4.33 in the circuit of the present invention for the same value of peak-to-peak ripple current in the output circuit as compared to a forward converter operating over the same range of input voltage and duty cycles.

Further examination of the circuit of the present invention reveals an additional important property. By connecting capacitor 44 with a value of C_{S1} and capacitor 46 with a value of C_{S2} across transistors 34 and 36, it is possible to delay the rise of the voltage across the switches at turn-off until the current in the switch reaches zero, thereby virtually eliminating turn-off losses.

Furthermore, by delaying the turn-on of the transistors until the load current is clamped by the body diodes (or diodes connected in parallel to the switches in case devices other then MOSFETS are used), the capacitors across the devices are charged/discharged by the load current, thereby eliminating the turn on losses of the switches.

In order to achieve these operating conditions, some constraints must be imposed on the circuit's elements.

For one optimized performance, the following constraints apply:

$$I_{L_{ptp}} = I_{mag_{ptp}} = \frac{Vin_{min} D_{max} . T}{L} = 2I'o_{max} \quad (13)$$

This equation allows calculation of L_{mag}:

$$L_{mag} = L = \frac{Vin_{min} D_{max} T}{2I'o_{max}} \quad (14)$$

where $I'o_{max}$ is the value of the output current reflected to the primary of the transformer 30. This constraint will bring the magnetizing current of transformer 30 to change between zero and $2I'o_{max}$ (ref. Fig. 4a) at full load and between $-Io'_{max}$ and $+Io'_{max}$ at no load.

As shown in Figures 4b and 4c, the current in Q_1, transistor 34 at the turn-off instant may vary from $I'o_{max}$ at no load to $3I'o_{max}$ at full load, while the current in Q_2, transistor 36 at turn off will be always equal to $I'o_{max}$. These circuits will be available to charge/discharge capacitors 44 and 46 during the dead time intervals between the transistors conduction.

Figure 4d shows the current of the primary winding 82 of transformer 30.

Figures 5a and 5b show the voltage at point A of Fig. 3 at no load and full load respectively. Since the lowest currents occur at no load, guaranteeing that the primary current of the transformer can charge the capacitors at no load during the available dead time, the constraints on the values of the capacitors and the dead time are determined by the no load condition:

$$I'o_{max} \cdot t_d = (C_{S1} + C_{S2}) \Delta V_{max} \cdot \quad (15)$$

where t_d is dead time between the conduction of transistors 34 and 36 and ΔV_{max} is the maximum peak to peak value of voltage at point A of Figure 3, the value of this voltage is given by:

$$\Delta V_{max} = [Vin(\frac{1}{1-D})]_{max} \quad (16)$$

Evidently, this value depends on the range of input voltage and the maximum duty cycle.

For an input voltage range of 2 and a maximum duty cycle of 0.7, ΔV_{max} will occur at minimum input voltage and will be equal to 3.333 Vin_{min}.

Equation 15 allows us to choose arbitrarily either the value of the capacitors or the value of the dead time t_d. For instance, when operating at a high frequency it may be desirable to use the drain-to-source capacitance of the transistors themselves to obtain zero voltage switching.

By substituting the value of the capacitances in Equation 15 we can find the value of t_d necessary to guarantee zero voltage switching. On some occasions the value of self-capacitance or parasitic capacitance of transistors 34 and 36 may be such that capacitors 44 and 46 are not necessary. The converter may still operate with zero switching losses using the self capacitance of transistors 34 and 36. Also, by making the peak-to-peak magnetizing current of the transformer either higher or lower than twice the reflected load current (Equation 13), we either increase the conduction losses in the switches and the primary of the transformer, or lose the zero voltage switching before reaching full load. Nevertheless, economic and other trade offs may dictate a relaxation of these constraints so only part of the potential improvement is realized.

It should be understood that by applying circuit theory rules to the configurations of Figures 1a, 2a and 3b, those versed in the art can modify the circuits without altering its topological essence or its mode of operation. For instance, by using two primary windings 60 and 62, as shown in Fig. 6, the circuit can be modified so that both switches are referred to the same point.

Fig. 7 illustrates another embodiment of the present invention. Specifically, the output circuit includes two separate inductors 70 and 72 each having a value L/2 which is one half the value of inductor 10 of Fig. 1a. Inductors 70 and 72 are connected in series with diodes 74 and 76. A capacitor 78 is connected between the common terminal of the inductors and the common terminal of the diodes. Hence, the output circuit provides full wave rectification by using two rectifiers 74 and 76 and a capacitor 78. The output voltage across the load in Fig. 7 is only one half the value of the voltage V_o obtained by the output circuit of Fig. 2a. An advantages of the output circuit of Fig. 7 is the use of only two rectifiers instead of a full bridge rectifier. Another advantage is the use of the inductors 70 and 72 as both flyback converter inductor and output filter inductors for the output voltage. The output circuit is similar to the circuit disclosed in U.S. patent No. 4,899,271 issued to Seiersen and incorporated herein by reference.

Fig. 8 illustrates another embodiment of the invention. The output circuit includes two separate inductors 82 and 84 each having a value L/2 which is one half the value of inductor 10 of Fig. 1a. Inductors 82 and 84 each have isolation windings 82a and 84a. Inductors 82 and 84 each have low magnetizing inductance. The isolation windings 82a and 84a are connected in series with diodes 80 and 86 connected at each end of the isolation windings. A capacitor 88 is connected between the common terminal of the isolation windings and the common terminal of the diodes. Load 90, is connected in parallel with capacitor 88. Hence, the output circuit provides full wave rectification by using two rectifiers 80 and 86 and a capacitor 88. The output circuit provides the benefits of isolation and voltage conversion, without the requirement of center tapping as is done in output circuits shown in Fig. 3b and Fig. 6. It should be appreciated that the topology of output circuit illustrated in Fig. 8 can be independently utilized in many applications with full-wave rectification and isolation.

As the foregoing demonstrates the present invention offers the significant advantages beyond those supplied by the prior art. Thus in addition to low voltage stress on the switching devices, wide duty cycle range and zero voltage switching at all load conditions, the present invention provides a significant reduction of output ripple as compared to cited prior art.

Claims

1. A DC to DC converter comprising:

an input voltage source;
energy storage inductance;
a capacitance;
at least one switching circuit for connecting said inductance alternatively across said input voltage and across said capacitance;
full wave rectification circuit for rectifying the resulting voltage across said inductance;
a filter circuit connected to filter said rectified voltage in order to generate a DC output voltage;
a control circuit for controlling the operation of said switching circuit for modulating said DC output voltage.

2. The converter of claim 1, wherein said filter circuit further comprises a filter inductor and a filter capacitor.

3. The converter of claim 1, wherein said switching circuit comprises two switching devices, the first switching device when closed connecting said energy storage inductance across said input voltage and said second switching device when closed connecting said energy storage inductance across said capacitance.

4. The converter of claim 3 wherein said control circuit drives said two switching devices such that (a) said first switching device is turned on while second switching device is off; (b) said first switching device is turned off and both said switching devices are off for a short dead-time interval; (c) said second switching device is turned on and said first switching device is off; (d) said second switching device is turned off and both said switching devices are off again for a short dead time interval; and (e) the process is repeated periodically.

5. The converter of claim 4 further comprising capacitance in parallel with at least one of said switching devices, so that voltage across said switching device is virtually zero prior to turning on or off.

6. The converter of claim 5 wherein said capacitance comprise self-capacitance of said electronic switching devices.

7. In a DC to DC converter having: an input voltage source; a capacitance coupled to said input voltage source; and an inductance, a method for regulating output power comprising the steps of:
connecting said inductance alternatively across said input voltage source and across said capacitance via a switching circuit;
full wave rectifying the resulting voltage across said inductance;
filtering said rectified voltage in order to generate a DC output voltage;
controlling the operation of said switching circuit for modulating said DC output voltage.

8. The method of claim 7, wherein said filtering step includes the step of providing said rectified voltage to a filter inductor and a filter capacitor.

9. The method of claim 8, wherein the step of connecting said inductance alternatively includes:
coupling two switching devices across said inductance;
closing the first switching device to connect said energy storage inductance across said input voltage source; and
closing the second switching device to connect said energy storage inductance across said capacitance.

10. The method of claim 9, wherein said step of controlling the switching circuit includes the steps of:
turning on said first switching device while said second switching device is off;
turning off said first switching device while said second switching device is off for a short dead-time interval;
turning on said second switching device while said first switching device is off;
turning off said second switching device while said first switching device is off for a short dead time interval;and
(e) repeating steps (a) through (d) periodically.

11. The method of claim 9 further comprising the step of reducing voltage across said switching devices to virtually zero prior to turning on or off by coupling capacitance in parallel with said switching devices.

12. A DC to DC converter comprising:
an input voltage source;
a capacitance;
an output circuit;
a switching circuit for connecting said output circuit alternatively across said input voltage source and said capacitance;
said output circuit further comprising:
an inductance coupled to the output of the switching circuit and having at least one rectifier at each end, the second terminal of said rectifiers coupled to a common point, and a capacitance and a load terminal connected across an intermediate point of said inductance and said common point.

13. The converter of claim 12, wherein said inductance comprises a first and a second inductance coupled in series forming said intermediate point.

14. A DC to DC converter comprising:
an input voltage source;
a capacitance;
an output circuit;
a switching circuit connecting said output circuit alternatively across said input voltage source and said capacitance;
said output circuit further comprising:
a first and second inductance coupled in series to the output of the switching circuit;
a third and fourth inductance coupled in series and formed by isolation windings across said first and second inductance, said third and fourth inductance having at least one rectifier at each end for full wave rectification, the second terminal of said rectifiers coupled to a common point, and a capacitance and a load terminal connected across an intermediate point of said third and fourth inductance and said common point.

15. In a DC to DC converter an output circuit comprising:
a first and second inductance coupled in series to form the first and second terminals of said output circuit;
a third and fourth inductance coupled in series and formed by isolation windings across said first and second inductance, siad third and fourth inductance having at least one rectifier at each end for full wave rectification, the second terminal of said rectifier coupled to a common point, and a capacitance and a load terminal connected across an intermediate point of said third and fourth inductance and said common point.

16. The converter of any one of claims 12 to 15, wherein said first and second inductance are substantially equal in value.

17. The converter of claim 14, wherein said third and fourth inductance are substantially equal in value.

18. The converter of claim 17, wherein said inductances have substantially low magnetising inductance.

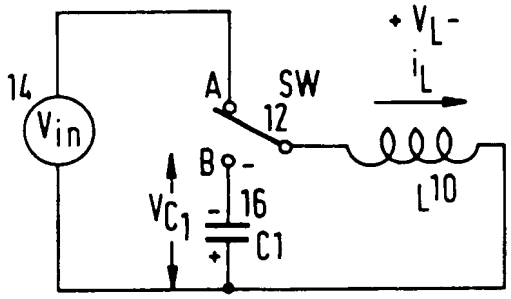
19. The converter of any one of claims 12 to 18, wherein said circuit comprises two electronic switching devices, the first switching device when closed connecting said output circuit across said input voltage source and said second switching device when closed connects said output circuit across said capacitance.

20. The converter of claim 19, wherein said switching circuit switches said two switching devices such that (a) said first switching device is turned on while said second switching device is off; (b) said first switching device is turned off and both said switching devices are off for a short dead-time interval; (c) said second switching device is turned on and said first switching device is off; (d) said second switching device is turned off and both said switching devices are off again for a short dead time interval; and (e) the process is repeated periodically.

21. The converter of claim 20 further comprising capacitance in parallel with at least one of said switching devices, so that voltage across said switching device is virtually zero prior to turning on or off.

22. The converter of claim 21 wherein said capacitance in parallel with said switching devices comprise self-capacitance of said electronic switching devices.

FIG. 1a



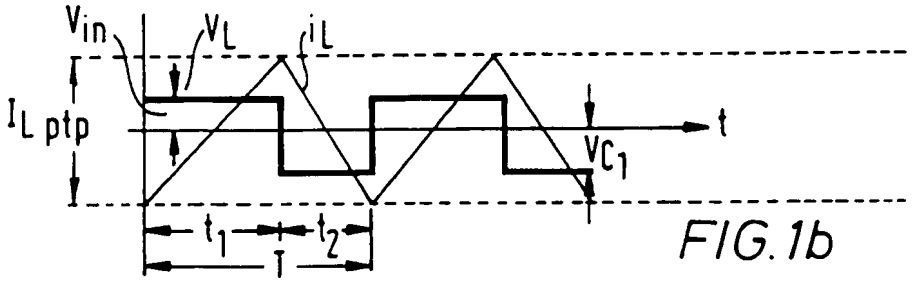


FIG. 1b

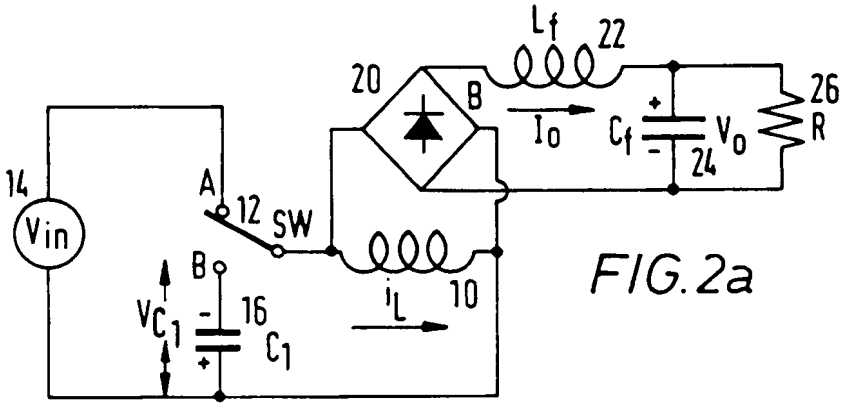


FIG. 2a

FIG. 2b

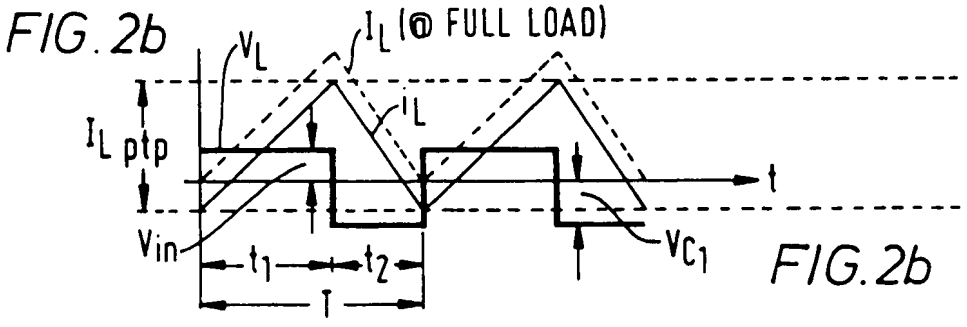
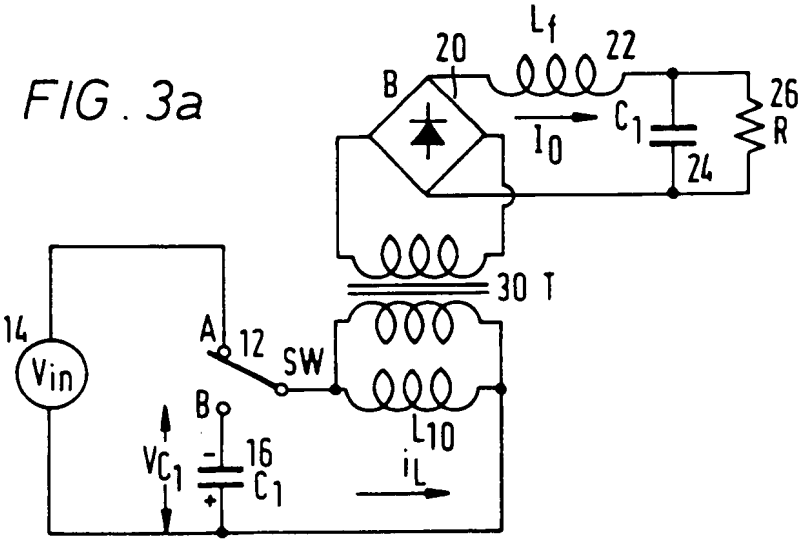


FIG. 2b

FIG. 3a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22
B
26
R
I_O
C_1
24
30 T
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A
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B
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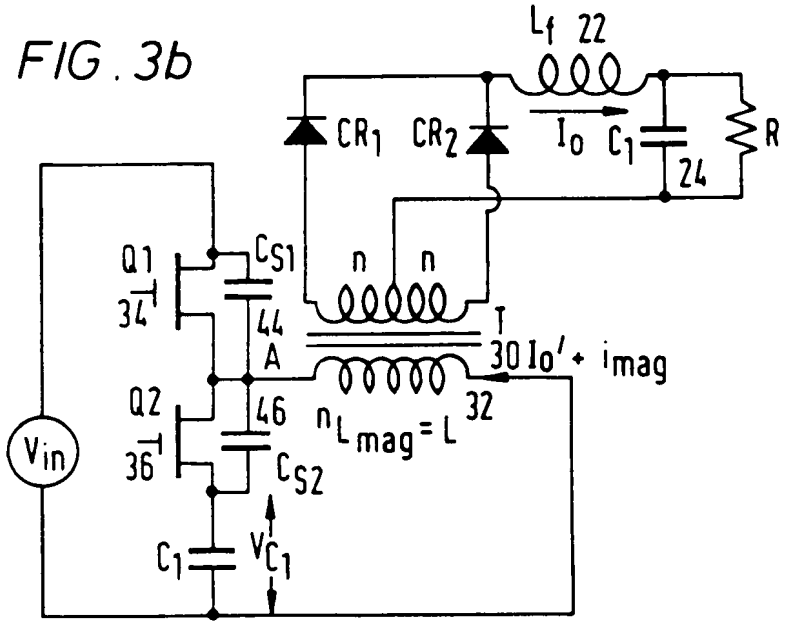
V_{C_1}
16
C_1
i_L

FIG. 3b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n
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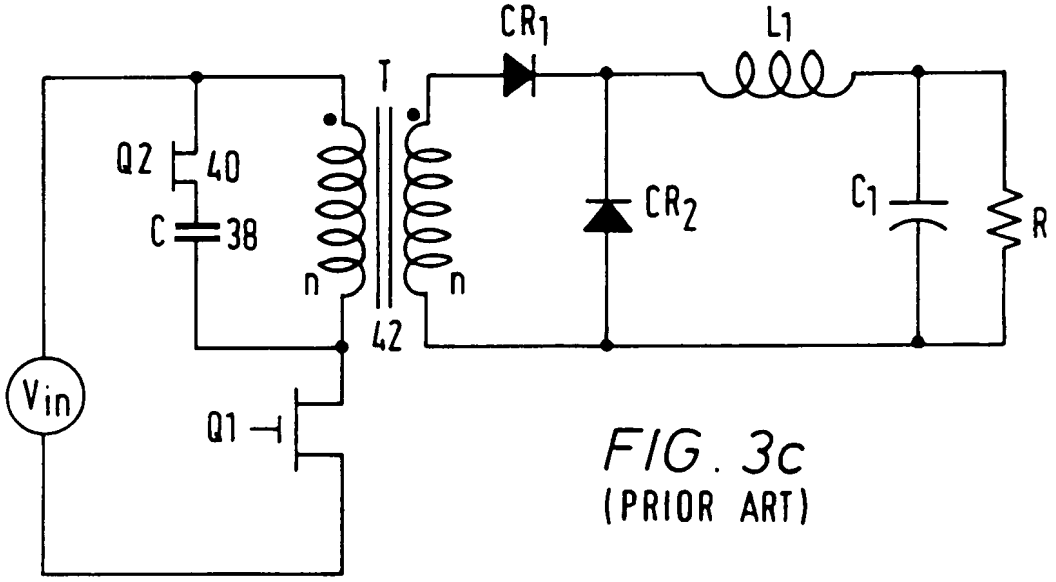


FIG. 3c
(PRIOR ART)

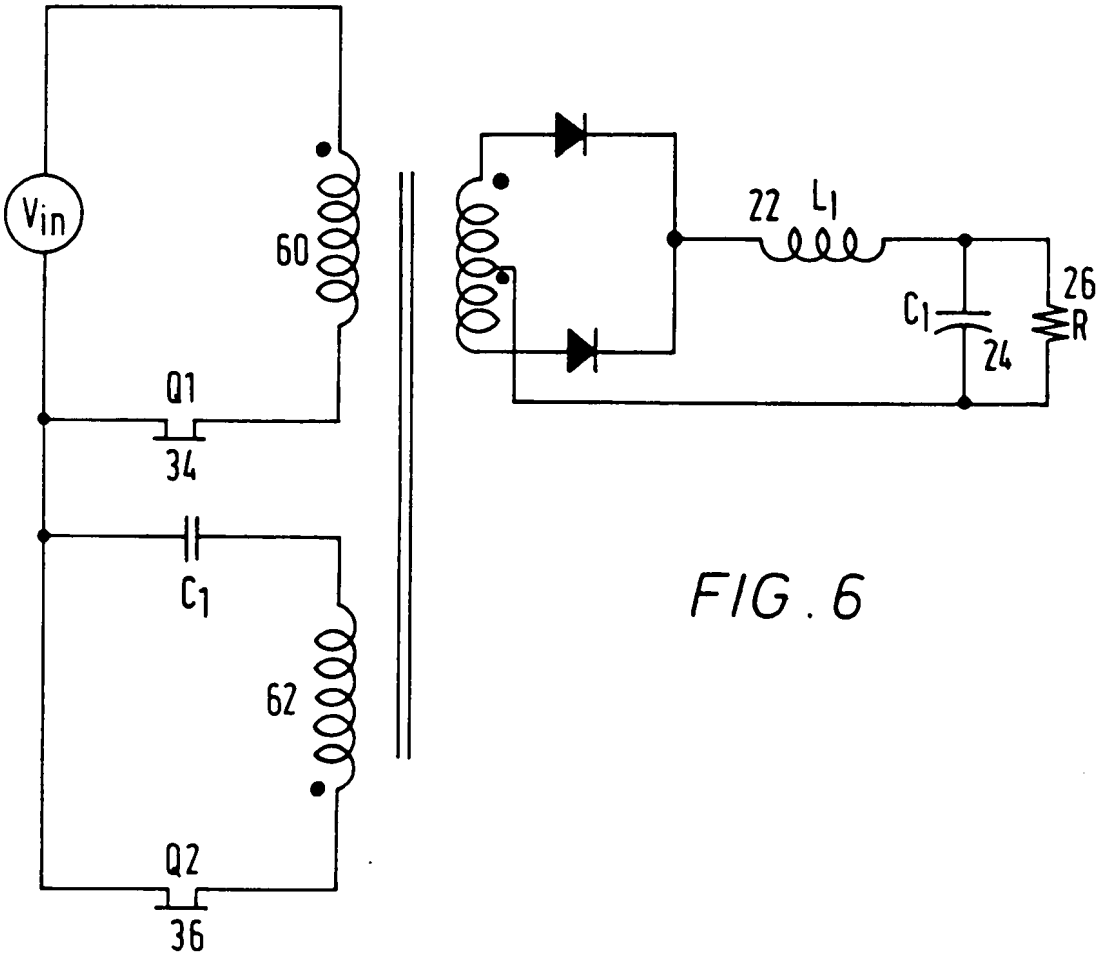
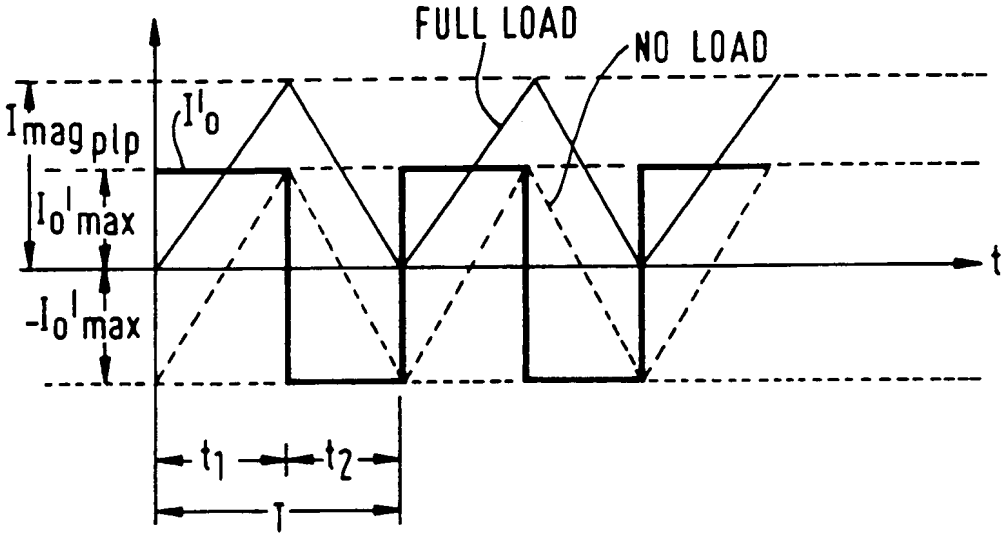


FIG. 6

FIG. 4a


FULL LOAD
NO LOAD
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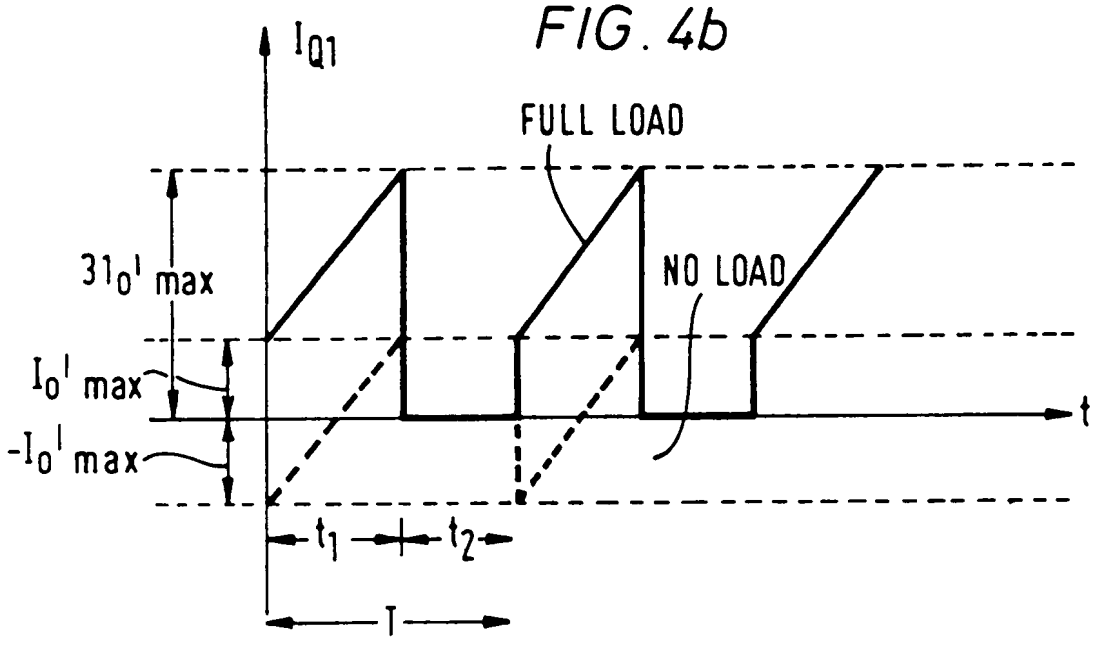
I'_o
$I_o{}'_{max}$
$-I_o{}'_{max}$
t
t_1
t_2
T

FIG. 4b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FULL LOAD
NO LOAD
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$-I_o{}'_{max}$
t
t_1
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T

FIG. 4c

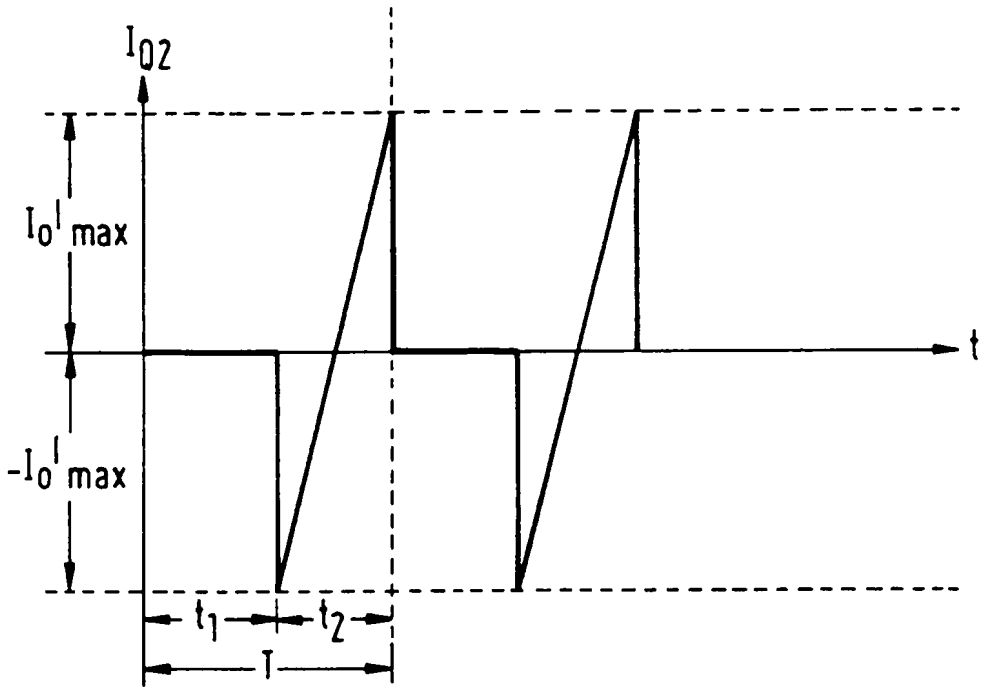


FIG. 4d

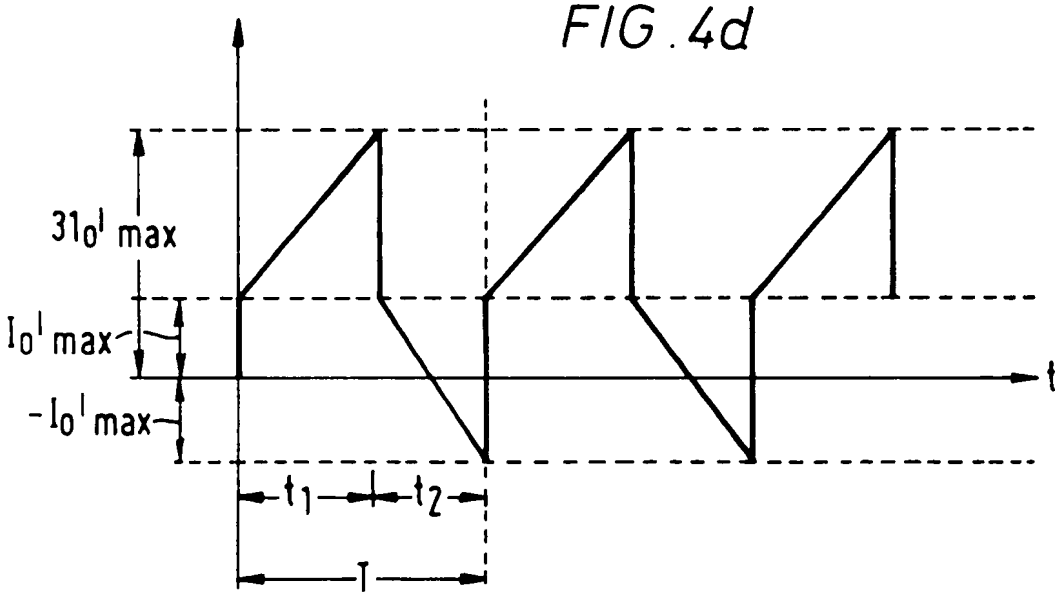


FIG. 5a

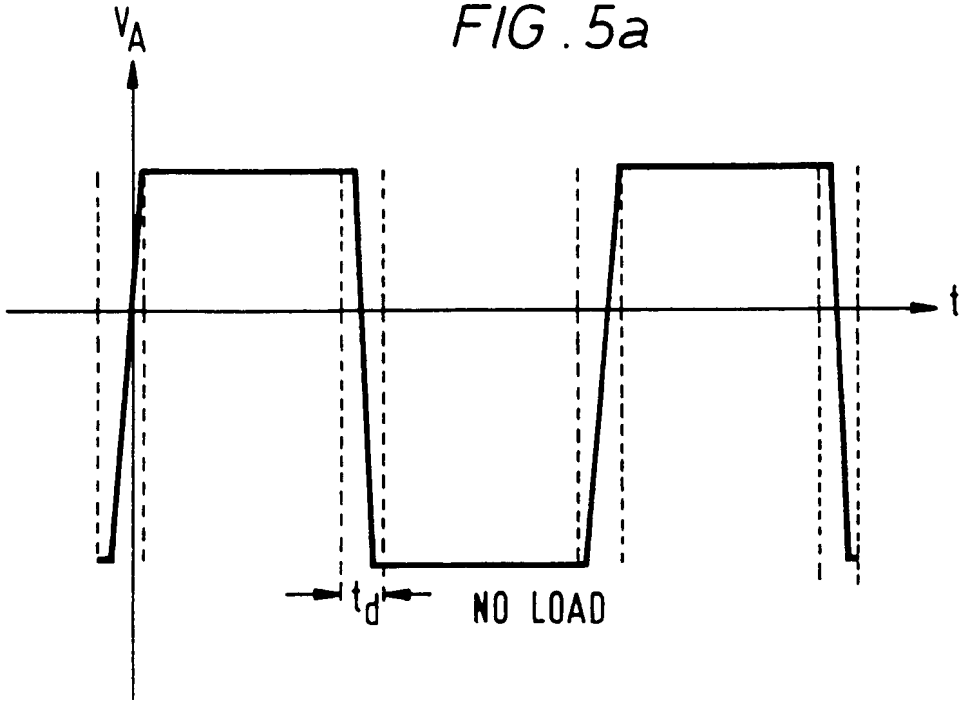


FIG. 5b

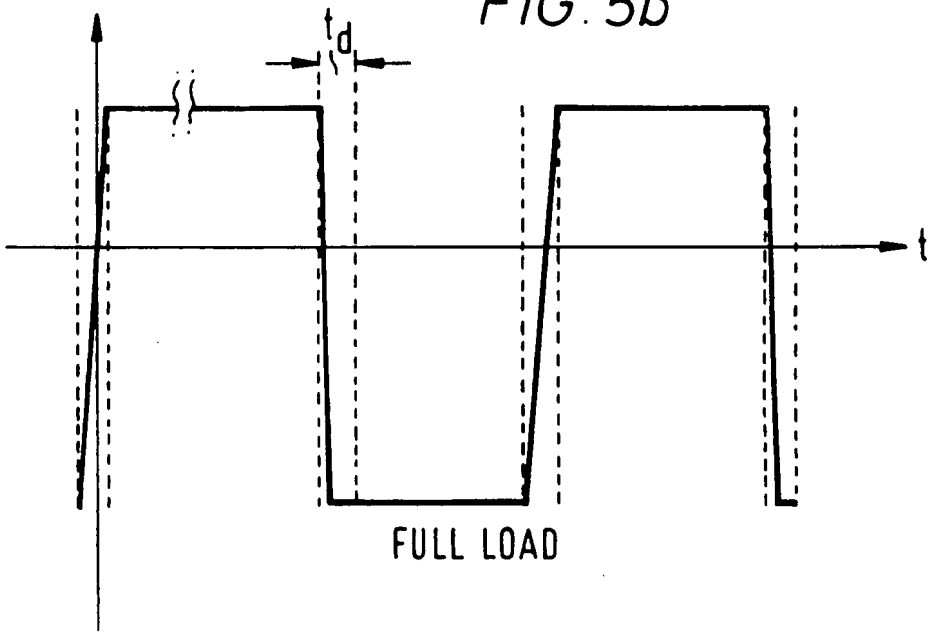


FIG. 7

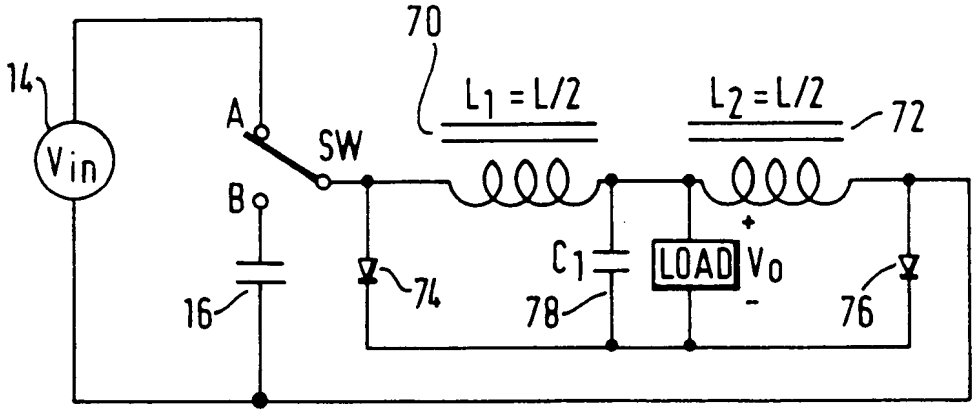
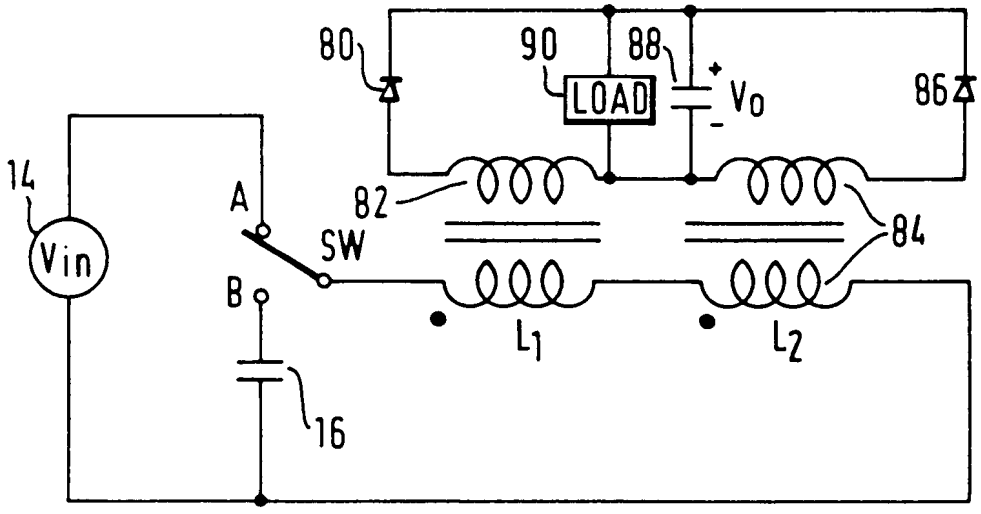

70
14
Vin
A
SW
B
16
L1 = L/2
L2 = L/2
72
74
C1
78
LOAD
Vo
76

FIG. 8


80
90
88
LOAD
Vo
86
14
Vin
A
SW
B
16
82
84
L1
L2

European Patent Office

EUROPEAN SEARCH REPORT

Application Number EP 92302818.7

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	WO - A - 89/08 347 (BLACK & DECKER) * Abstract; page 4, lines 22-34; page 6, line 31 - page 7, line 19; claims 1,2, 6,8,9,10; fig. 1,3 *	1,3,4, 7,9, 10,12, 13,14	H 02 M 3/337
D,A	US - A - 4 959 764 (BASSETT) * Column 5, lines 12-56; claims 1,2,3,4; fig. 5 *	1,2,3, 4,7,8, 9,10, 14	
A	EP - A - 0 289 196 (AMERICAN TELEPHONE AND TELEGRAPH COMPANY) * Page 3, line 52 - page 4, line 6; claim 1; fig. 2 *	1,2,3, 4,5,6, 7,8,9, 10,12, 13,14	
D,A	US - A - 4 809 148 (BARN) * Column 4, lines 37-58; claims 1,2,3,4,5,6,10,11; fig. 8,11 *	1,2,3, 4,5,7, 8,9, 10,14	TECHNICAL FIELDS SEARCHED (Int. Cl.5) H 02 M
D,A	US - A - 4 618 919 (MARTIN) * Column 2, lines 23-41; claims 1,3,5,8,9; fig. 1 *	1,3,4, 7,9, 10,14	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	24-07-1992	MEHLMAUER

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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